



MINNESOTA NANOCENTER

Microfabrication Teaching Laboratory

Option 2: Making a MOSFET

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Microfabrication Teaching Laboratory

The Minnesota Nano Center, University of Minnesota

Option 2: Making a MOSFET

Overview. This lab introduces students to the processes involved with fabricating micro devices, such as integrated circuits and micromechanical systems. Students reproduce the fabrication steps used in optical lithography, using simplified tools to carry out thin film deposition, patterning, etching, doping, and characterization. By following the procedure, students should be able to produce working examples of p - n junction-based devices, and perform electronic tests on these devices.

The MOSFET lab is based on the materials and processes outlined in Microfabrication Teaching Laboratory Option 1—Making a Diode. It is recommended that the instructor explore the Option 1 activity first before attempting the MOSFET lab, in which students fabricate a set of working field effect transistors (FETs) starting from a bare silicon wafer. More specifically, students build metal oxide semiconductor FETs (MOSFETs), on which the majority of current digital electronic devices are based.

The MOSFET activity is divided into six sections.

Section 1: wafer cleaning and oxide growth. Students start with bare silicon wafers, clean them to remove fingerprints and dust, then use a high temperature furnace to grow an oxide layer on the wafers.

Section 2: layer 1 fabrication. Students print several photomasks on plastic film, spin-coat the wafer with photoresist (PR), expose the PR-covered wafer using the photomask and a light source, and develop the PR to yield a patterned wafer. They then use an etchant chemical to remove the exposed areas on the patterned wafer.

Section 3: doping. The active regions of the device are formed by adding phosphorus in a liquid suspension to the wafer surface and driving the dopant into the exposed silicon regions using high heat.

Section 4: fabrication of the gate, source, and drain regions. Students use additional patterning and etching steps to fashion the three terminal contacts for the MOSFET device.

Section 5: finishing the transistor. Students apply a metal paste to form three contact terminals (source, drain, and gate) of the finished device..

Section 6, device testing. A simple current-voltage (I-V) is used to test the performance of the MOSFET device.

Time Required

Prior to lab: Wafers must be oxidized by firing them for 14 hours. With temperature ramp-up and cool down, allow for 24 hours to prepare the oxidized wafers.

Patterning, etching, and doping: Two to three hours.

Post doping heat treatment: About four hours are required to heat wafers and then cool to room temp.

Gate fabrication: This requires five steps. The only substantial time required is that for growing the thin gate oxide; about four hours are required to heat wafers and then cool to room temp.

Final device assembly: About two hours.

Device testing: About one hour.

Level: Undergraduate students. An introduction to solid state physics, particularly *p-n* junctions and the theory of transistor operation, is required. Some familiarity with acid-base chemistry is desirable.

Resources Needed

Standard Lab Equipment

- One or more hotplates, preferably with temperature readouts, preset to 105°C
- A lab oven capable of maintaining 140°C
- One 500mL beaker for mixing developer solution
- Four shallow trays to hold developer, etching bath, acetone, and water baths. Trays should be wide enough to immerse a 100mm wafer. Plastic food storage containers may be used.
- Three photomasks, one for each of the fabrication layers
- One or more desk lamps with a compact fluorescent bulb (20-25W recommended)
- Optical microscope, preferably with digital camera
- Tweezers
- Digital timer
- Splash-proof safety goggles
- Chemical safety gloves

Special Equipment. See Appendices 1 and 2 for sources and for plans on how to build low cost tools for the lab.

- Tube furnace, large enough to accept 100mm wafers and capable of attaining 1100 C
- Quartz tube for the furnace
- Spin coater
- Clear plastic containment box, about 45x30x25 cm
- Current-voltage tester

Consumable Materials

- Gloves, light duty (for general wafer handling)
- Deionized water
- A source of clean, dry, particle-free compressed air
- Lint-free laboratory wipes
- Disposable plastic droppers
- Kapton tape or similar for masking the silver paste

Special materials, solvents, and chemicals. See Appendix 1 for sources. Note safety guidelines below.

- Solvents: methanol, acetone, isopropyl alcohol
- Silicon wafers, pre-cleaned, 100mm diameter, doped p-type
- Photomasks (3): see Appendix 2 for designs.

- Photoresist: Microposit S1813. This must be stored in a dark-colored plastic bottle.
- Developer for the photoresist: Microposit 351. Dilute this concentrate by mixing one part 351 with 5 parts deionized or distilled water.
- Etchant: Rust Stain Remover (3% HF solution in water)
- Spin-on n-type dopant
- Conductive silver epoxy, for applying contacts to the device.

Safety

- Splash-proof safety goggles and light duty gloves are required when handling solvents, photoresist, and wafers.
- Heavier chemical-resistant gloves are needed for the etch chemical, which is a 3% solution of hydrofluoric acid. Concentrated HF can cause serious burns; this more dilute solution is safer to handle, but still requires the use of splash-proof chemical goggles and heavy gloves designed for caustic chemical handling (i.e., not light latex gloves). Wipe up spills immediately.
- Avoid contact with photoresist; use soap and water to remove any material that touches skin.
- The developer solution contains sodium hydroxide and is alkaline. Wear plastic gloves when handling.
- Solvents and the photoresist must be handled with adequate air circulation to avoid buildup of solvent vapor. Use of chemical fume hoods is recommended, but a well-ventilated laboratory is acceptable.
- Safety Data Sheets for the chemicals used above are available at <http://www.msds.com>.
- These chemicals must be stored, used, and disposed of safely following your organization's chemical hygiene and hazardous waste disposal procedures.
- Use care when handling silicon wafers; they are fragile and may shatter into sharp fragments if dropped.

Procedure

Section I. Growing the oxide layer

In this section the wafers to be processed have a thin film of oxide grown on their surface. This is done by heating the silicon wafer to 1050°C in air, which creates a layer of silicon dioxide (SiO₂) about 350-400 nm thick that will function as an insulator.

1. Place the wafers to be coated on a clean surface. If the wafers are not brand new, clean them by squirting a small quantity of isopropanol on each wafer and gently wiping with a dust-free wipe.
2. Place the wafers inside the quartz tube which is placed in the tube furnace.
3. Set the tube furnace temperature controls at 1050°C. Expose the wafer to this temperature for 14-16 hours to grow the oxide layer.
4. Shut down the furnace and allow the wafers to cool at least four hours.
5. Remove the wafers from the furnace and visually inspect them. Estimate the thickness of the silicon oxide layer by comparing wafer color to the oxide color chart. The wafers should have oxide layers of roughly 3500Å (350nm).

Section II. First Layer Fabrication

In this section the top oxide layer of the wafer is patterned using photoresist, and the wafer is etched. At the end of this step, the pattern from the mask will have been transferred to the wafer.

1. Pre-clean the Wafer

- a. Place wafers on a dry, clean wipe. Squirt a small quantity of isopropanol on each wafer and gently wipe with a clean room wipe. Allow the alcohol to dry from the wafers
- b. Blow-dry the front of the wafers with particle-free compressed air.
- c. Place the wafers on the hotplate set at 105°C for 60 seconds to drive off any remaining alcohol. Allow to cool.

2. Apply Photoresist

- a. Place the spinner inside the containment box. Line the box with paper towels to catch excess photoresist.
- b. Place a wafer on the spinner so that the flat of the wafer is next to a peg on the spinner disk. Rotate the wafer so that its outer edge is under all three pegs.
- c. Position the spinner so that its center is directly under the hole in the lid of the containment box. Place the lid on the box to check alignment, and adjust if needed. With the lid on, turn the spinner on and allow it to run about 30 seconds to reach full speed.
- d. While the spinner is spinning up to speed, open the bottle of photoresist. Withdraw enough photoresist into a disposable dropper to fill about 2-3 cm up from the bottom of the dropper tip.
- e. When the spinner has reached full speed, insert the dropper into the hole in the box lid. Try to position the dropper directly over the center of the spinning wafer.

- f. Squirt all the photoresist in the dropper onto the wafer in one continuous motion (i.e., don't stop and start but apply all the dropper contents at once to achieve an even coating). Allow the spinner to run 30 seconds, then shut it off and allow the spinner to spin down.
- g. Place the wafer on the hotplate set at 105°C for 60 seconds. This helps to drive off excess solvent and prepare the photoresist for imaging.
- h. Allow the wafer to cool for 1-2 minutes. Keep the wafers out of direct sunlight and strong room light during this time.

3. Expose and develop the photoresist

- a. Place the wafer on a non-reflective surface.
- b. Place photomask 1 directly on the wafer. The side on which the pattern is printed should be in the down position, closest to the wafer surface.
- c. Position the compact fluorescent bulb about 12 cm above the mask.
- d. Expose the wafer for 3 minutes.
- e. Submerge the wafer in the developer solution and agitate for 45-60 seconds.
- f. Submerge the wafer in deionized water for 1-2 minutes.
- g. Dry the wafers using compressed air.
- a. Inspect the wafer to ensure that the pattern was transferred accurately. If not, remove the photoresist by immersing the wafer in acetone. Rinse the wafer in isopropanol, then repeat steps 1-3

4. Hard Bake

- a. The photoresist is relatively weakly bonded to the underlying oxide layer. When the wafer is immersed in the etching bath, the etchant will often diffuse under the photoresist and lift it off the wafer surface, causing an uncontrolled etch and degrading the pattern.
- b. To prevent this, the wafer must be "hard-baked". Place the wafer in a lab oven set to 140°C, and allow the wafer to bake for 20 minutes. This bonds the photoresist more completely to the wafer surface and should prevent any photoresist lift-off.

5. Etching. After the wafer is patterned with photoresist, it is ready for etching. Areas of exposed oxide are removed using a dilute solution of hydrofluoric acid. The HF solution requires the use of gloves and splash proof safety goggles.

- a. Add the 3% HF solution to a plastic tray. DO NOT use a glass container for holding or storing the HF solution.
- b. Place the patterned wafer in the HF solution. Leave the wafer in the etching solution for 25 to 30 minutes. The tray should be kept covered during this time to minimize evaporation.
- c. At 10 minute intervals, observe the surface of the wafer in the etch bath. The photoresist may exhibit a pattern of cracking, but should remain on the wafer. If the resist appears to be coming off the wafer surface in flakes, the etch may be compromised and the sample may be over-etched. Withdraw the wafer and start over.
- d. After 25 minutes, withdraw the wafer from the etch bath, place in a water bath, and agitate gently. Then rinse the wafer under running water.
- e. Test for etching completion: observe how water wets the surface of the wafer. Bare silicon is hydrophobic, and water should readily de-wet from a completely etched surface. The oxide is more hydrophilic, so water should evenly wet and sheet the oxide-covered regions.
- f. Dry the wafer using compressed air.
- g. Estimate the thickness of the oxide-covered regions using the SiO₂ film thickness color chart. They should be in the 1800 to 2500 Å range.

We have now etched open two holes per transistor. These will form the *source* and *drain* regions of the MOSFET after they are doped in the next section.

Section III. Doping

In this step the source and drain regions on the p-type wafer that were exposed by the previous etching step are coated with an n-type dopant (phosphorus). When exposed to high temperature, the phosphorus atoms diffuse into the silicon, creating *p-n* junctions at the source and drain which are needed to make the transistor.

1. Apply the spin-on dopant.
 - a. With the spinner inside the containment box, place the wafer on the spinner and attach it to the spinner as described in step II.2.b above.
 - b. Position the spinner so that its center is directly under the hole in the lid of the containment box. With the lid on, turn the spinner on and allow it to run about 30 seconds to reach full speed.
 - c. While the spinner is reaching running speed, fill a plastic pipette with about one ml of spin-on dopant.
 - d. When the spinner has reached full speed, insert the dropper into the hole in the box lid. The dropper should be positioned directly over the center of the spinning wafer.
 - e. Apply the dopant in the dropper onto the wafer in one continuous motion. Allow the spinner to run 30 seconds, then shut it off and allow the spinner to spin down.
 - f. Remove the wafer from the spinner.
 - g. Place the wafer on a hot plate at 200°C for 15 minutes to remove excess solvent from the wafer.
2. Drive in the dopant at high temperature
 - a. The dopant must be driven into the bulk silicon using high temperatures to speed up diffusion.
 - b. Set the tube furnace temperature controls at 1030°C.
 - c. Place the wafer in a ceramic holder and have a quartz rod available with which to insert the wafer holder into the hot furnace
 - d. When the tube furnace has reached temperature, slowly and carefully insert the wafer carrier into the furnace using the quartz rod. Full safety equipment (goggles and heavy insulating gloves) must be used for this step. The wafer carrier must be inserted slowly (~3 cm/minute) to avoid thermal stresses on the wafers or carrier.
 - e. Once the wafer carrier has been fully inserted into the furnace, leave it at 1030°C temperature for 1-2 hours to diffusively drive the phosphorus dopant into the open areas on the wafer.
 - f. After 1-2 hours, shut down the furnace and allow the wafers to cool at least three hours.
3. Since the dopant spread out over the whole wafer but does not need to be present on the oxide-covered areas, it needs to be etched from the latter.
 - a. Place the wafer in the 3% HF bath for a few minutes to cleanup these areas.
 - b. Rinse the wafer in DI water.
 - c. Dry using compressed air or allow to air dry.

Section IV. Gate Fabrication

The gate region of a MOSFET consists of a very thin layer of oxide which acts as an electrical insulator. To make this layer, we have to pattern a new layer on the wafer, remove the existing (too thick) oxide film from the area where the gates will be, then re-grow a very thin oxide layer by placing the wafer briefly in a hot tube furnace. The final step uses a third photomask to apply a pattern to the wafer, which is then etched again to re-open contacts to the source and drain regions of the MOSFET.

1. Fabricate the second layer of the wafer, repeating the relevant steps from Section II above.
 - a. Clean the wafer, repeating step 1 from Section II.
 - b. Using photomask 2, pattern layer 2 by repeating steps 2 and 3 under Section II. Inspect the pattern.
 - c. Hard bake the photoresist (follow step 4 under Section II above).
 - d. Etch layer 2 by repeating step 5 of Section II. This removes the unneeded thick oxide layer over the gate region.

2. Re-grow a thin gate oxide layer for the MOSFET gates.
 - a. Set up the tube furnace and place the wafer in the carrier.
 - b. Place the wafer in the furnace and set the temperature for 1030°C
 - c. Fire the wafer for 30 minutes.
 - d. Turn off the furnace and allow the wafer to cool.
 - e. Check the thickness of the gate oxide by reference to the oxide color chart. The color should be greyish-black, indicating 500-1000 Å.

3. Fabricate the third layer of the wafer, repeating the relevant steps from Section II above.
 - a. Clean the wafer, repeating step 1 from Section II.
 - b. Using photomask 3, pattern layer 3 by repeating steps 2 and 3 under Section II.
 - c. Hard bake the photoresist (follow step 4 under Section II above).
 - d. Etch layer 3 for 4 minutes. This removes the oxide layer over the source and drain regions, re-opening them so we can connect them to electrical leads later. The source and drain regions should appear hydrophobic when water is applied.

Section V. Finishing the Transistor

The wafer now contains many copies of a MOSFET transistor. To test these devices, we must apply metal contacts to the transistor terminals (the source, drain, and gate). This is done by applying a conductive metal paste to the terminals that allow probes to be placed on the device.

1. Clean the doped wafer with acetone and DI water and wipe it thoroughly.
2. Using the two-part silver epoxy, carefully apply a small amount to the source, gate, and drain regions, taking care not to connect them.
3. While the epoxy is still wet, insert a 5cm copper wire into each dab of epoxy. Hold it still while the epoxy cures (about 15 minutes).
4. When the epoxy is dry, cover the contact with hot glue to strengthen the lead connection and also insulate.
5. Follow directions on the metallic paste as to drying. When dry, the device is ready to test.

Section VI. Device Characterization

The MOSFETs made in this lab are characterized in terms of their current-voltage response, i.e., the I-V curve. Forward and reverse voltages are applied to the junction and the resulting current measured.

To test the I-V curve of the devices made in this activity, we recommend the ADAL M1000 tool from Analog Devices. With the aid of a simple external circuit, the M1000 can measure the I-V curve from diodes and transistors; it can collect the data, graph the results, and allow quantitative measurements of turn-on voltage, leakage current, and breakdown voltage.

Information on how to set up the circuit and use the M1000 can be found at Analog Devices' web site, wiki.analog.com/university/tools/m1k. See Appendix I for ordering information.

APPENDIX 1. Sources for materials and equipment

Materials

- Solvents may be obtained from Fisher Scientific (www.fishersci.com), Sigma Aldrich (www.sigmaaldrich.com), or other academic chemical supply houses.
- P-type silicon wafers may be obtained from several sources, including Polishing Corp of America (www.pcasilicon.com) and University Wafer (www.universitywafer.com). Wafers come in many grades; for this activity, specify p-doped test grade wafers. At this writing (spring 2017) these wafers cost about \$12 each when purchased in quantities of 25.
- The Microposit 1813 photoresist and Microposit 351 developer can be ordered from MicroChem Corp., Newton, MA; tel: 617-965-5511, e-mail: sales@microchem.com. One liter of the photoresist costs about \$160 at this writing, which should supply at least 100 experiments.
- The etchant in this activity is a commercial product called Rust Stain Remover, available in hardware and home improvement stores, and directly from the manufacturer at www.whink.com.
- The spin-on p-type dopant used here is Phosphorofilm made by Emulsitone Chemicals, LLC. Order at Emulsitone.com.
- To make the electrical contacts, use silver conductive epoxy from Ted Pella, Inc. (tedpella.com), product #16043.

Equipment

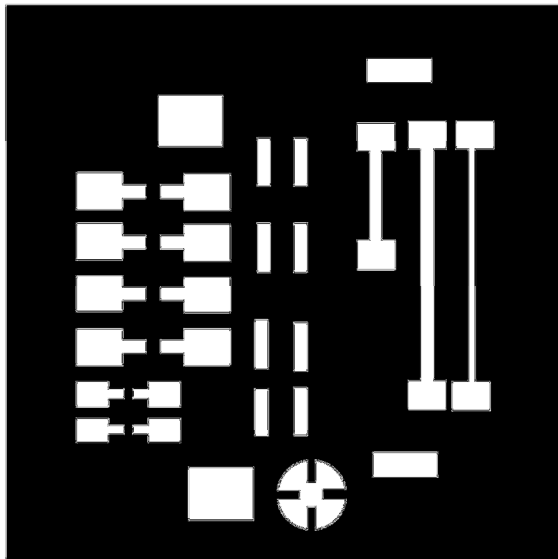
- Spin coater. A simple device for spin coating photoresist may be constructed from a 120VAC 3" cooling fan with a 4" aluminum or plastic plate attached to the fan blades. Plans and a parts list for building the fan motor-based spin coater may be obtained from the Nano Center at the University of Minnesota, Minneapolis, MN. Call 612 624-8005 for more information.
- Containment box. Suitable clear plastic containment boxes may be found in the housewares section of a hardware store or similar outlets.
- Photomasks. See the instructions and designs in Appendix 2 to create the photomasks for this lab.
- Current-voltage tester. The devices made in this activity can be tested using the ADAL M1000 tool from Analog Devices. With the aid of a simple external circuit, the M1000 can measure the I-V curve from diodes and transistors. More information can be found at wiki.analog.com/university/tools/m1k. Ordering information is at: www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/ADALM1000.html#eb-overview.
- Tube furnace and tube may be ordered from Fisher Scientific (www.fishersci.com), Sigma Aldrich (www.sigmaaldrich.com), or other academic supply houses. The tube must be large enough to accept 100mm wafers, which means the furnace cost may be over \$5000.

As an alternative to a laboratory tube furnace, an art clay ceramics kiln may be used. Remove all pottery debris and try to clean the loose ceramic powder inside the kiln, then place the silicon wafers on a ceramic support and fire to the cone corresponding to about 1100°C (2012°F).

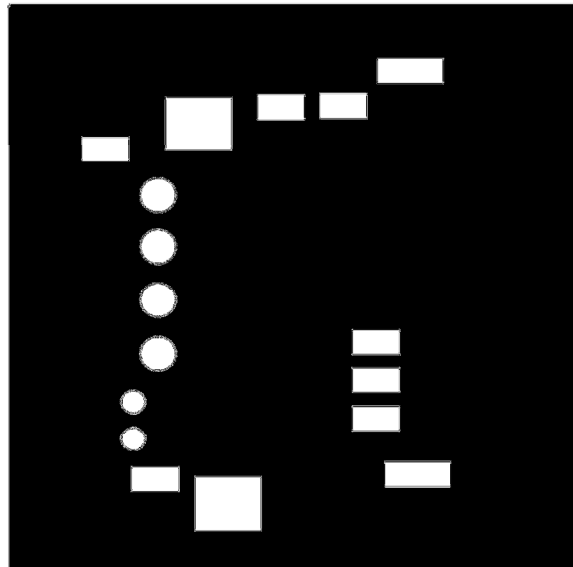
APPENDIX 2. Photomask Templates

Create these photomasks on polyester transparency film using a high quality xerographic copier or inkjet or laser printer. When using some printers to produce these transparencies, the pattern may be insufficiently opaque to ensure a clean masking effect. To obtain a fully opaque pattern with an inkjet printer, simply repeat the print on the same sheet of transparency. A good quality office xerographic printer should require only two passes; ink jet printers tend to require additional layers to get an opaque image. If needed, five overprinting passes can be done on an ink jet printer without serious image degradation, as long the paper guides are carefully aligned. Allow the ink to dry fully (at least five minutes) between passes.

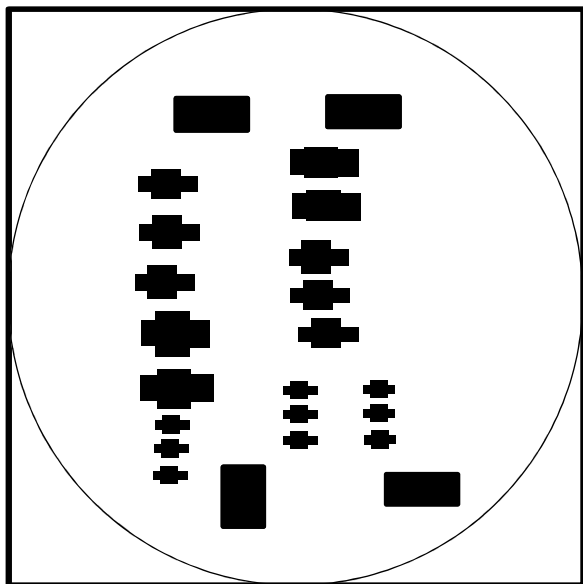
Photomask 1



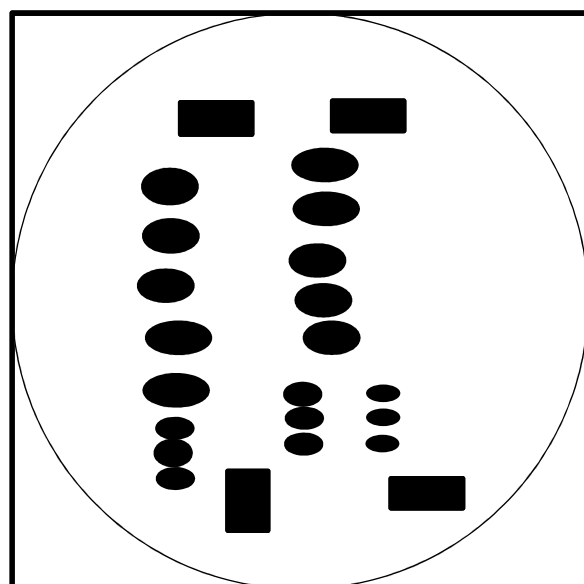
Photomask 2



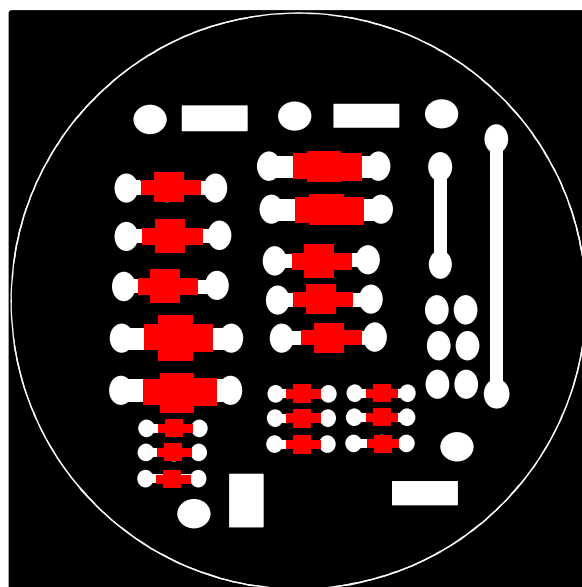
Photomask 3A



Photomask 3B



Overlap of mask patterns



APPENDIX 3. Silicon Dioxide color card

Thin films of silicon dioxide will exhibit different colors according to how thick the layer is. Thus, the appearance of the oxide formed on silicon wafers is a guide to the thickness of the oxide layer. Use the color chart below to gauge the thickness of the oxide layer on your wafers.

| SiO ₂ Thickness Color Chart | |
|--|--|
| Film Thickness (Å) | Color of Film (those shown are only indicative) |
| 500 | tan |
| 700 | brown |
| 1000 | dark violet to red violet |
| 1200 | royal blue |
| 1500 | light blue to metallic blue |
| 1700 | metallic to very light yellow-green |
| 2000 | light gold or yellow - slightly metallic |
| 2200 | gold with slight yellow-orange |
| 2500 | orange to melon |
| 2700 | red-violet |
| 3000 | blue to violet-blue |
| 3100 | blue |
| 3200 | blue to blue-green |
| 3400 | light green |
| 3500 | green to yellow-green |
| 3600 | yellow-green |
| 3700 | green-yellow |
| 3900 | yellow |
| 4100 | light orange |
| 4200 | carnation pink |
| 4400 | violet-red |
| 4600 | red-violet |
| 4700 | violet |
| 4800 | blue-violet |
| 4900 | blue |
| 5000 | blue-green |
| 5200 | green |
| 5400 | yellow-green |
| 5600 | green-yellow |
| 5700 | yellow to "yellowish" (at times appears light gray or metallic) |
| 5800 | light orange or yellow to pink |
| 6000 | carnation pink |
| 6300 | violet-red |
| 6800 | "bluish" (appears between violet-red and blue-green - overall looks grayish) |
| 7200 | blue-green to green |
| 7700 | "yellowish" |
| 8000 | orange |
| 8200 | salmon |
| 8500 | dull light red-violet |
| 8600 | violet |
| 8700 | blue-violet |
| 8900 | blue |
| 9200 | blue-green |
| 9500 | dull yellow-green |
| 9700 | yellow to "yellowish" |
| 9900 | orange |